National Semiconductor™

FPD-Link Demonstration Kit User Manual

P/N FLINK3V8BT-85

Preliminary Rev 1.0

Interface Products

Table of Contents

Introduction:

National Semiconductor - Interface Products Group FPD-Link evaluation kit contains a Transmitter (Tx) board, a Receiver (Rx) board along with interfacing cables. This kit will demonstrate the chipsets interfacing from test equipment or a graphics controller using Low Voltage Differential Signaling (LVDS) to a receiver board.

The Transmitter board accepts LVTTL/LVCMOS RGB signals from the graphics controller along with the clock signal. The LVDS Transmitter converts the LVTTL/LVCMOS parallel lines into four serialized LVDS data pairs plus a LVDS clock. The serial data streams toggle at 3.5 times the clock rate.

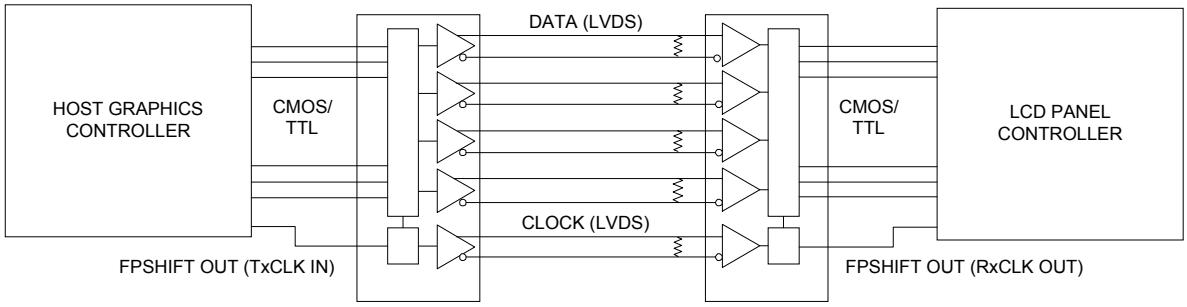
The Receiver board accepts the LVDS serialized data streams plus clock and converts the data back into parallel LVTTL/LVCMOS RGB signals and clock for the panel timing controller.

The user needs to provide the proper RGB inputs and clock to the Transmitter and also provide a proper interface from the Receiver output to the panel timing controller or test equipment. A cable conversion board or harness scramble may be necessary depending on type of cable/connector interface used. A power down feature is also provided that reduces current draw when the link is not required.

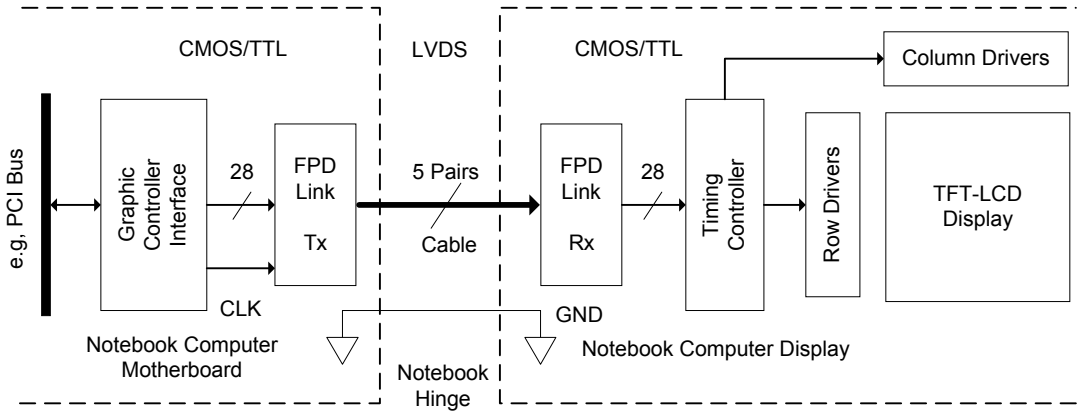
Contents of the Evaluation Kit:

1) One Transmitter board with the DS90C385MTD - 28 bit Transmitter
2) One Receiver board with the DS90C386MTD - 28 bit Receiver
3) One 20-pin IDC Flat Ribbon Cable
4) One 60-pin IDC Flat Ribbon Cable
5) Evaluation Kit Documentation (this manual)
6) DS90C385/386 Datasheet
7) LVDS Owner's Manual (2nd Edition)

FPD-Link Typical Application:



FPD-Link Application



Typical FPD-Link Application (24-bit Color)

The diagrams above illustrate the use of the Chipset (Tx/Rx) in a Host to LCD Panel Interface.

Chipsets support up to 18-bit or 24-bit AM-TFT LCD Panels for any VGA (640X480), SVGA (800X600), XGA (1024X768), and Single/Dual Pixel SXGA (1280X1024) resolutions.

Because of the non-periodic nature of STN-DD SHFCLK, the Chipset may not work with all D-STN panels. The PLL CLK input of the Transmitter requires a free running periodic SHFCLK. Most Graphics Controller can provide a separate pin with a free running clock. In this case the STN-DD SHFCLK can be sent as Data while the free running clock can be used as SHFCLK for the PLL ref CLK. For example, C&T's 65550's WEC (Pin 102) can be programmed to provide a free running clock using the BMP (Bios Modification Program). Please refer to STN Application using (AN-1056) for more information on STN support.

Refer to the proper datasheet information on Chipsets (Tx/Rx) provided on each board for more detailed information.

How to set up the Evaluation Kit:

The PCB routing for the Tx input pins (TxIN) have been laid out to accept incoming data from a 60-pin IDC connector. The TxOUT/RxIN interface uses a 20-pin IDC connector through a IDC ribbon cable. Please follow these steps to set up the evaluation kit for bench testing and performance measurements:

1) Connect one end of the 20-pin IDC cable to the transmitter board and the other end to the receiver board. Longer lengths can be used.

Note: Previous HSL Tx/Rx 8 Bit boards have different IDC pinouts and must be scrambled in the IDC cable in order to be compatible with this demo kit.

2) Jumpers have been configured at the factory, they should not require any changes for operation of the chipset. See text on Jumper settings for more details.
3) From the Graphics card, connect a flat (ribbon) cable to the transmitter board and connect the another flat cable from the receiver board to the panel (Note: Refer to AN-1127 for suggested mapping schemes). Note that pin 1 on the connector should be connected to pin 1 of the cable. A scramble cable may be required.
4) Power for the Tx and Rx boards must be supplied externally through TP1 (Vcc). Grounds for both boards are connected through TP2 (GND) (see section below).

Power Connection:

The Transmitter and Receiver boards must be powered by supplying power externally through TP1 (Vcc) and TP2 (GND) on EACH board. The maximum voltage that should ever be applied to the FPD-Link Transmitter (385) or Receiver (386) Vcc terminal is +4V MAXIMUM.

FPD-Link Transmitter Board Description:

J1 (60 position) accepts 28 bit LVTTL/LVCMOS data along with the clock.

The FPD-Link Transmitter board is powered externally. For the transmitter to be operational, the Power Down pin must be set HIGH with a jumper. Rising or falling edge reference clock is selected by JP1 tied to Vcc (rising) or GND (falling).

The 20-pin IDC connector (J2) provides the interface for LVDS signals for the Receiver board.

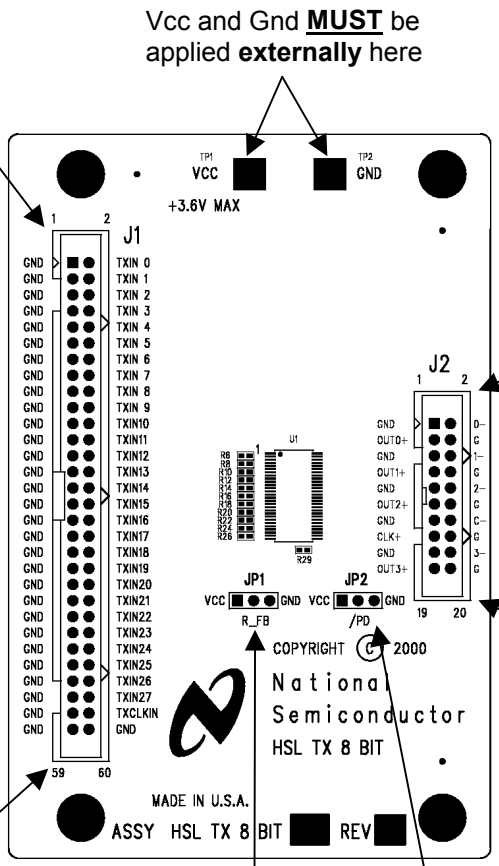
Note: Previous HSL Tx/Rx 8 Bit boards have different IDC pinouts and must be scrambled in the IDC cable in order to be compatible with this demo kit.

60-pin IDC Connector

1	2
GND	**TXIN0**
GND	**TXIN1**
GND	**TXIN2**
GND	**TXIN3**
GND	**TXIN4**
GND	**TXIN5**
GND	**TXIN6**
GND	**TXIN7**
GND	**TXIN8**
GND	**TXIN9**
GND	**TXIN10**
GND	**TXIN11**
GND	**TXIN12**
GND	**TXIN13**
GND	**TXIN14**
GND	**TXIN15**
GND	**TXIN16**
GND	**TXIN17**
GND	**TXIN18**
GND	**TXIN19**
GND	**TXIN20**
GND	**TXIN21**
GND	**TXIN22**
GND	**TXIN23**
GND	**TXIN24**
GND	**TXIN25**
GND	**TXIN26**
GND	**TXIN27**
GND	**TXCLKIN**
GND	*GND*

59 60

J1



TxOUT LVDS signals
20-pin IDC connector

1	2
GND	**OUT0-**
OUT0+	*GND*
GND	**OUT1-**
OUT1+	*GND*
GND	**OUT2-**
OUT2+	*GND*
GND	**CLK-**
CLK+	*GND*
GND	**OUT3-**
OUT3+	*GND*

19 20

J2

Note: Previous HSL Tx/Rx 8 Bit boards have different IDC pinouts and must be scrambled in the IDC cable in order to be compatible with this demo kit.

Jumper Settings for the Tx Board

Jumper	Purpose	Settings
R_FB (JP1)	**R**ising or **F**alling Data Strobe	 = Rising (Vcc GND)  = Falling (Vcc GND)

Default setting is JP1 set LOW (to GND), falling edge strobe.

/PD (JP2)	**P**ower**D**own	 = ON (Vcc GND (ON: Tx is operational;)  = OFF (Vcc GND OFF: Tx powers down)

Default setting is JP2 set HIGH (to Vcc), operational mode.

Tx LVDS Mapping by IDC Connector

The following two figures illustrate how the Tx inputs are mapped to the IDC connector (J1) (Note – labels are also printed on the demo boards). The 20-pin IDC (J2) connector pinout is also shown.

(Transmitter Board)

60-pin IDC Connector

Pin 1			
	GND	TXIN0	2
	GND	TXIN1	
	GND	TXIN2	
	GND	TXIN3	
	GND	TXIN4	
	GND	TXIN5	
	GND	TXIN6	
	GND	TXIN7	
	GND	TXIN8	
	GND	TXIN9	
	GND	TXIN10	
	GND	TXIN11	
	GND	TXIN12	
	GND	TXIN13	
	GND	TXIN14	
	GND	TXIN15	
	GND	TXIN16	
	GND	TXIN17	
	GND	TXIN18	
	GND	TXIN19	
	GND	TXIN20	
	GND	TXIN21	
	GND	TXIN22	
	GND	TXIN23	
	GND	TXIN24	
	GND	TXIN25	
	GND	TXIN26	
	GND	TXIN27	
	GND	TXCLKIN	
59	GND	GND	60

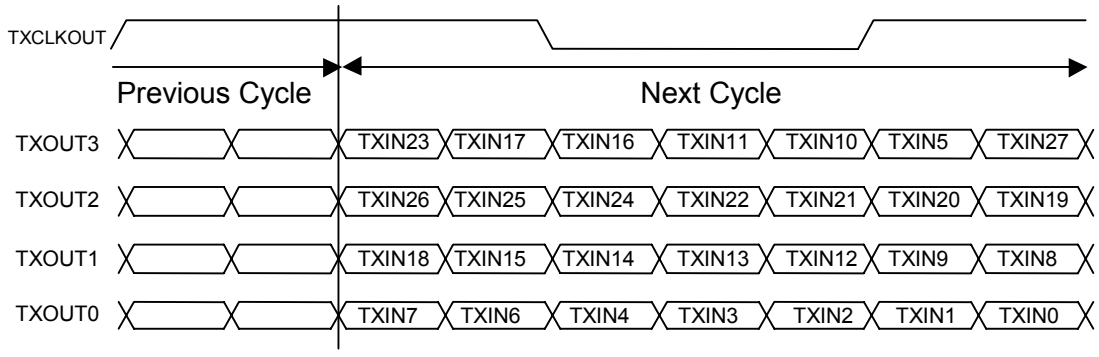
J1

TXOUT0
TXOUT0
TXOUT1
TXOUT1
TXOUT3
TXOUT1
TXOUT2
TXOUT2

TxOUT LVDS signals
20-pin IDC connector

Pin 1			
	GND	OUT0-	2
	OUT0+	GND	
	GND	OUT1-	
	OUT1+	GND	
	GND	OUT2-	
	OUT2+	GND	
	GND	CLK-	
	CLK+	GND	
	GND	OUT3-	
19	OUT3+	GND	20

J2



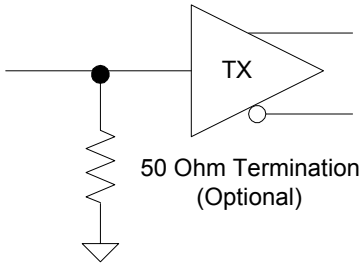
Parallel LVTTL/LVCMOS Data Inputs Mapped to LVDS Outputs

Tx Board Options: 50 Ohm Termination for TxIN

On the Tx demo board, the 29 inputs have an option for 50 Ohm terminations. There are 0402 pads for this purpose. One side is connected to the signal line and the other side is tied to ground. These pads are unpopulated from the factory but are provided if the user needs to install a 50 Ohm termination. R1 TO R28 are associated with the Tx data input lines. R29 is associated with CLKIN. Some test equipment may require a 50 Ohm load.

Mapping of Transmitter Inputs for the Optional Termination Resistors is shown below:

Tx Pin Names	Tx Pin Number	Termination Resistor
TxIN0	51	R1
TxIN1	52	R2
TxIN2	54	R3
TxIN3	55	R4
TxIN4	56	R5
TxIN5	2	R6
TxIN6	3	R7
TxIN7	4	R8
TxIN8	6	R9
TxIN9	7	R10
TxIN10	8	R11
TxIN11	10	R12
TxIN12	11	R13
TxIN13	12	R14
TxIN14	14	R15
TxIN15	15	R16
TxIN16	16	R17
TxIN17	18	R18
TxIN18	19	R19
TxIN19	20	R20
TxIN20	22	R21
TxIN21	23	R22
TxIN22	24	R23
TxIN23	25	R24
TxIN24	27	R25
TxIN25	28	R26
TxIN26	30	R27
TxIN27	50	R28
TxCLKIN	31	R29



BOM (Bill of Materials) Transmitter PCB:

HSL Demo Board Schematic REV3
HSL8TXR3 Revision: 3 FPD-Link

Item	Qty	Reference	Part	Pkg Size
1	1	C1	10 µF	CASE D
2	4	C2,C6,C10,C14	0.1 µF	1206 (3216)
3	4	C3,C7,C11,C15	22 µF	7343 (D)
4	3	C4,C8,C12	0.001 µF	0805 (2012)
5	3	C5,C9,C13	0.01 µF	0805 (2012)
6	2	JP2,JP1	3_PIN_HEADER	0.1" spacing
7	1	J1	IDC30X2	IDC60
8	1	J2	IDC10X2	IDC20
9	29	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24,R25,R26, R27,R28,R29	Optional (See previous page)	0402
10	8	R30,R31,R32,R33,R34,R35, R36,R37	0 Ohm	0402
11	2	TP1,TP2	N/A	TP_.2"X.2"
12	1	U1	DS90C385MTD	56-pin TSSOP

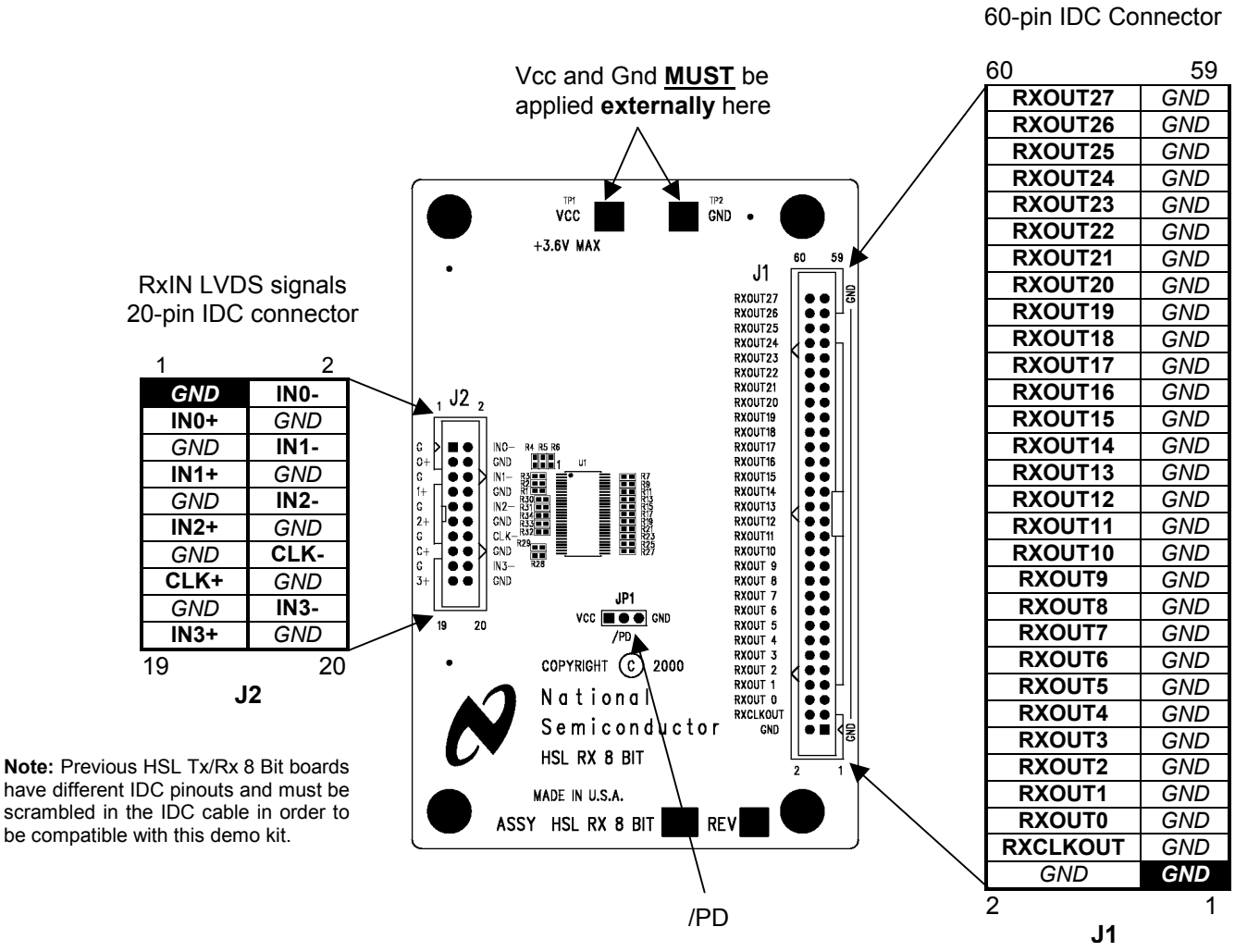
Rx FPD-Link Receiver Board:

J1 (60 position) provides access to the 28 bit LVTTL/LVCMOS and clock outputs.

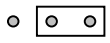
The FPD-Link Receiver board is powered from the pads show below. For the receiver to be operational, the Power Down pin must be set HIGH with the jumper.

The 20-pin IDC connector (J2) provides the interface for LVDS signals for the Receiver board.

Note: Previous HSL Tx/Rx 8 Bit boards have different IDC pinouts and must be scrambled in the IDC cable in order to be compatible with this demo kit.



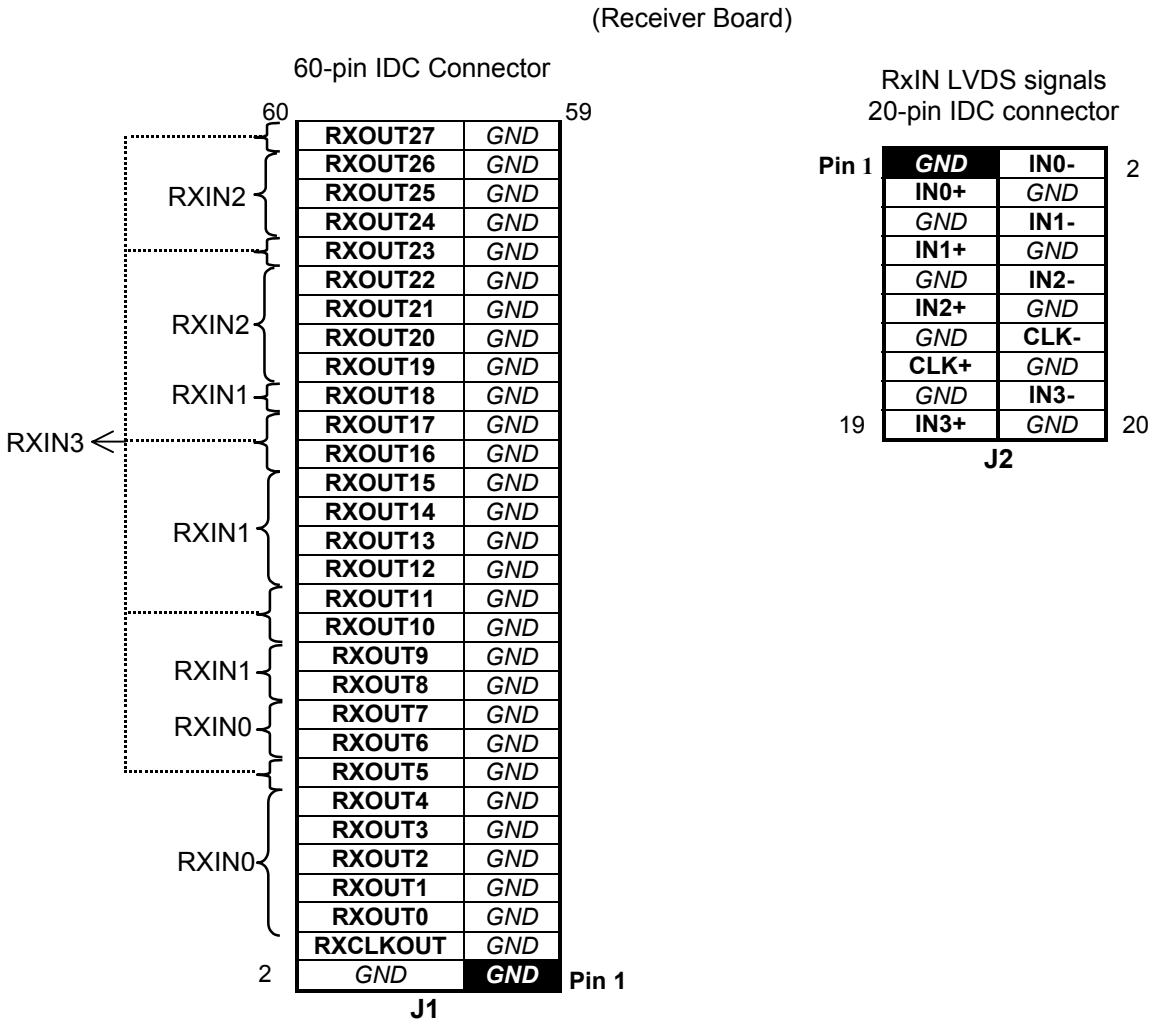
Selectable Jumper Settings for the Rx Board

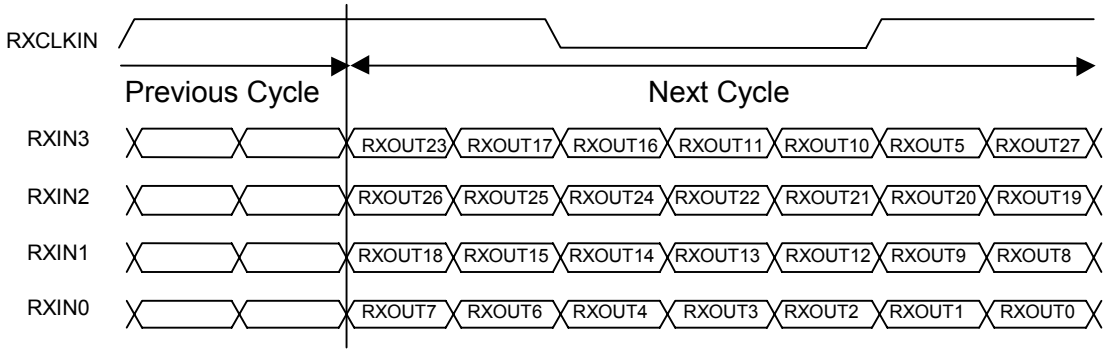
Jumper	Purpose	Settings	
/PD (JP1)	**P**ower**D**own	 = ON Vcc GND (ON: Rx is operational;	 = OFF Vcc GND OFF: Rx powers down)

Default setting is JP1 set HIGH (to Vcc), operational mode.

LVDS Mapping by IDC Connector

The following two figures illustrate how the Rx outputs are mapped to the IDC connector (J1) (Note – labels are also printed on the demo boards). The 20-pin IDC connector (J2) pinout is also shown.





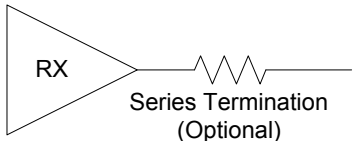
LVDS Data Inputs Mapped to LVTTL/LVCMOS Outputs

Rx Optional: Series Termination for RxOut

On the Rx demo board, there are 29 outputs that have an 0402 pad in series (which are shorted out). These pads are unpopulated from the factory but are provided if the user needs to install a 450 Ohm series resistors. This is required if directly connecting to 50 Ohm inputs on a scope. To use this option the user must cut the signal line between the pads before installing the 450 Ohm series resistors. R1 to R28 are associated with the DATA output lines. R29 is associated with CLKOUT. The total load presented to the receiver output is 500 Ohms (450 + 50). The waveform on the scope is 1/10 of the signal due to the resulting voltage divider (50 / (450 + 50)).

Optional Series Termination Resistor mapping is shown below:

Rx Pin Names	Rx Pin Number	Series Termination Resistor
RxOUT0	27	R28
RxOUT1	29	R27
RxOUT2	30	R26
RxOUT3	32	R25
RxOUT4	33	R24
RxOUT5	34	R23
RxOUT6	35	R22
RxOUT7	37	R21
RxOUT8	38	R20
RxOUT9	39	R19
RxOUT10	41	R18
RxOUT11	42	R17
RxOUT12	43	R16
RxOUT13	45	R15
RxOUT14	46	R14
RxOUT15	47	R13
RxOUT16	49	R12
RxOUT17	50	R11
RxOUT18	51	R10
RxOUT19	53	R9
RxOUT20	54	R8
RxOUT21	55	R7
RxOUT22	1	R6
RxOUT23	2	R5
RxOUT24	3	R4
RxOUT25	5	R3
RxOUT26	6	R2
RxOUT27	7	R1
RxCLKOUT	26	R29



BOM (Bill of Materials) Receiver PCB:

HSL Demo Board Schematic REV3
HSL8RXR3 Revision: 3 FPD-Link

Item	Qty	Reference	Part	Pkg Size
1	1	C1	10 µF	CASE D
2	4	C2,C6,C10,C14	0.1 µF	1206 (3216)
3	4	C3,C7,C11,C15	22 µF	7343 (D)
4	3	C4,C8,C12	0.001 µF	0805 (2012)
5	3	C5,C9,C13	0.01 µF	0805 (2012)
6	1	JP1	3_PIN_HEADER	0.1" spacing
7	1	J1	IDC30X2	IDC60
8	1	J2	IDC10X2	IDC20
9	29	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24,R25,R26, R27,R28,R29	Optional (See previous page)	0402
10	6	R35,R36,R37,R38,R39,R40	0 Ohm	0402
11	5	R30,R31,R32,R33,R34	100 Ohm	0402
12	2	TP1,TP2	N/A	TP_.2"X.2"
13	1	U1	DS90CF386MTD	56-pin TSSOP

Typical Connection / Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the TX inputs:

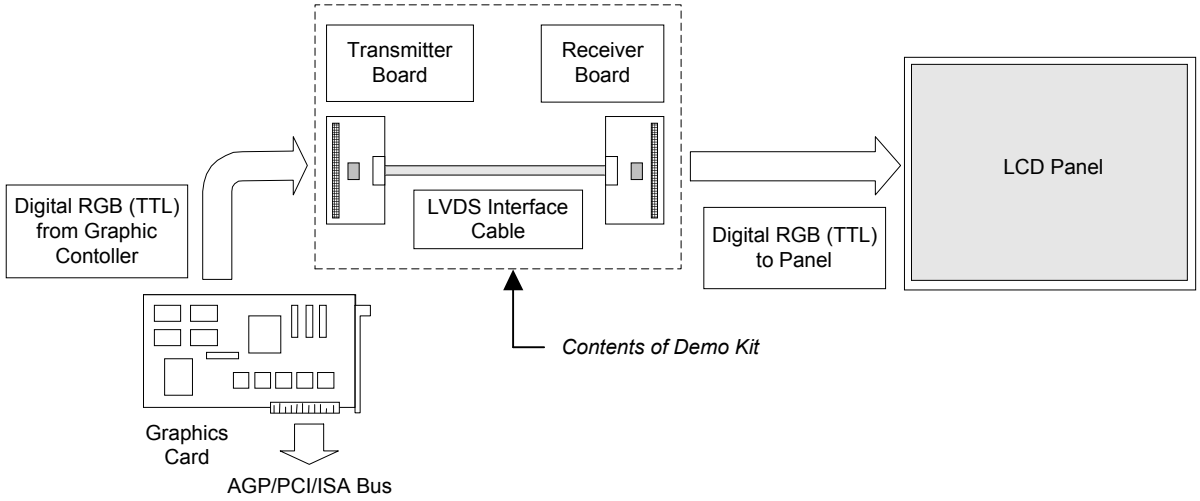
1) Graphics card or GUI controller with digital RGB (TTL) output.
2) TEK HFS9009 - This pattern generator along with 9DG2 Cards may be used to generate input signals and also the clock signal.
3) TEK DG2020 - This generator may also be used to generate data and clock signals.
4) TEK MB100 BERT - This bit error rate tester may be used for both signal source and receiver.
5) Any other signal / pattern generator that generates the correct input levels as specified in the datasheet.

The following is a list of typically test equipment that may be used to monitor the output signals from the RX:

1) LCD Display Panel which supports digital RGB (TTL) inputs.
2) TEK MB100 BERT - Receiver.
3) Any SCOPE with 50 Ohm inputs or high impedance probes.

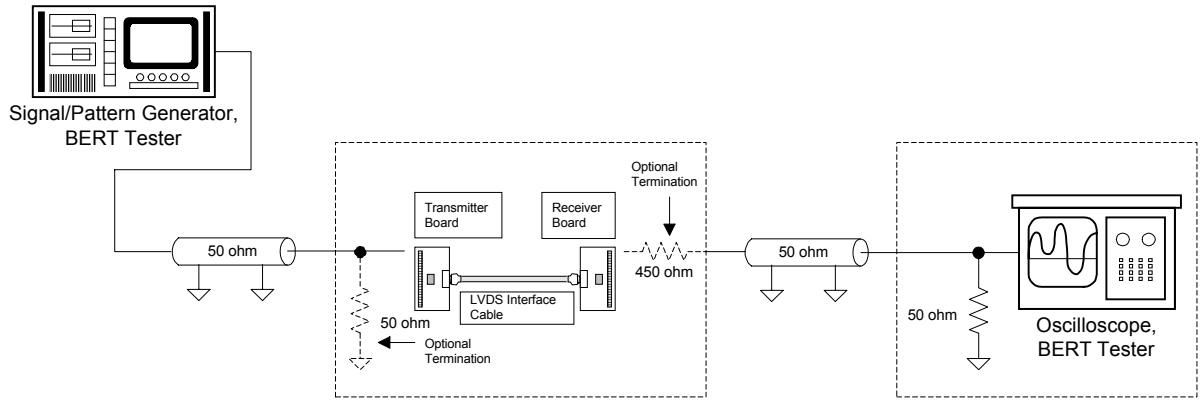
LVDS signals may be easily measured with high impedance / high bandwidth differential probes such as the TEK P6247 or P6248 differential probes.

The picture below shows a typical test set up using a Graphics Card and LCD Panel.



Typical FPD-Link Setup / PC Panel Application

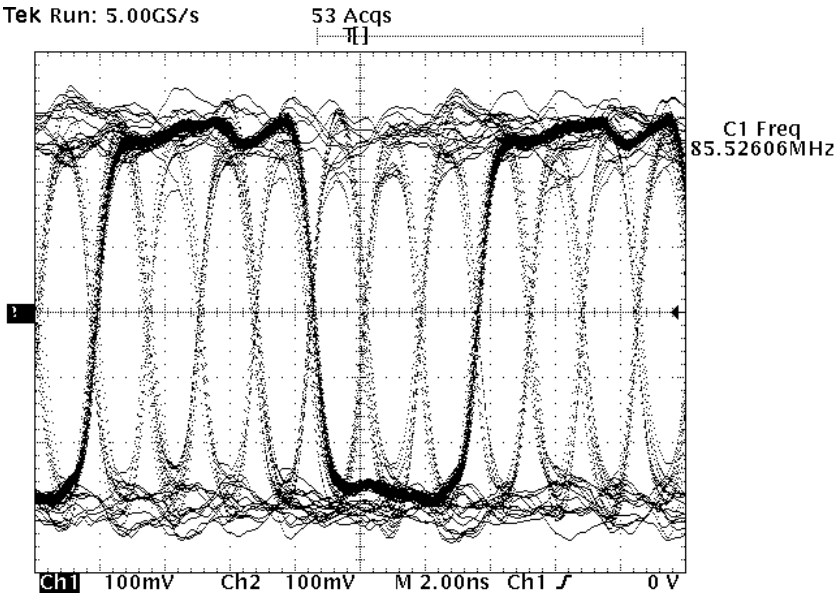
The picture below shows a typical test set up using a generator and scope.



Typical Connection / Test Equipment Setup

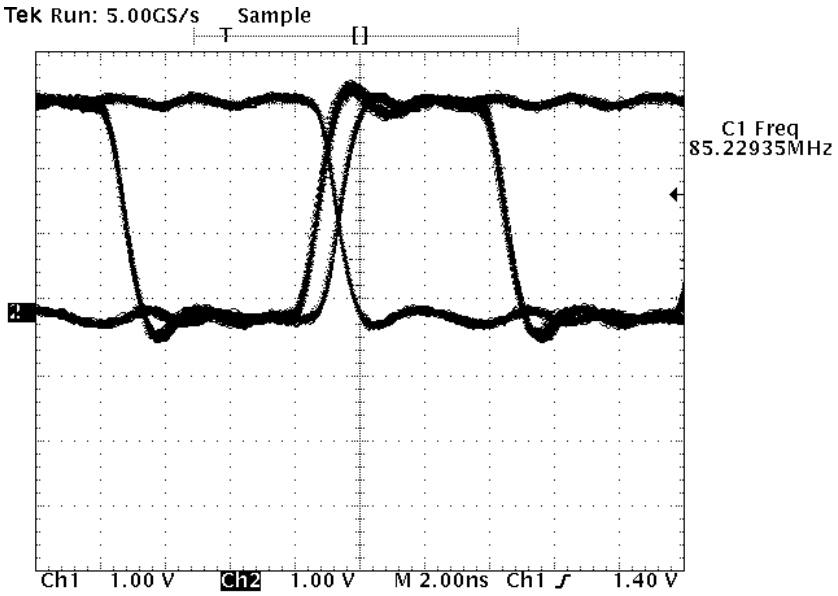
Typical Waveshapes

LVDS



The plot above shows both the LVDS Data channel with PRBS data and also the LVDS Clock over laid. Note that the clock pattern is 4 bit times HIGH and 3 bit times LOW. The differential signal should be typically +/-300mV. These waveforms were acquired using the TEK P6248 Probes. Clock rate is 85MHz.

RxOUT



The plot above shows both the recovered PRBS data and also the regenerated Clock overlaid. Note that the clock transitions slightly before the data transition and strobes the data on the falling edge of the clock. The data and clock signals are low drive 3V CMOS outputs. The plot above is at 85MHz.

Troubleshooting

If the demo boards are not performing properly, use the following as a guide for quick solutions to potential problems. If the problem persists, please contact the Interface Applications hotline number (+1 408 721 8500) for assistance.

QUICK CHECKS:

1. Check that Power and Ground are connected to both Tx AND Rx boards.
2. Check the supply voltage (typical 3.3V) and also current draw with both Tx and Rx boards (should be about 200mA with clock and one data bit at 66MHz).
3. Verify input clock and input data signals meet requirements (VIL, VIH, tset, thold), Also verify that data is strobed on the selected rising/falling (R_FB pin) edge of the clock.
4. Check that the Jumpers are set correctly.
5. Check that the cable is properly connected.

TROUBLESHOOTING CHART

Problem…	Solution…
There is only the output clock. There is no output data.	Make sure the data is applied to the correct input pin. Make sure data is valid at the input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly. Make sure that the cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both boards and make sure that the devices are enabled (/PD=Vcc) for operation.
The devices are pulling more than 1A of current.	Check for shorts in the cables connecting the TX and RX boards.
After powering up the demo boards, the power supply reads less than 3V when it is set to 3.3V.	Use a larger power supply that will provide enough current for the demo boards, a 500mA power supply is recommended.

Additional Information

For more information on FPD-Link Transmitters/Receivers, refer to the National's LVDS website at:

www.national.com/appinfo/fpd

Application Notes

- AN-1032 An Introduction to FPD-Link
- AN-1056 STN Application using FPD-Link
- AN-1059 High Speed Transmission with LVDS Devices
- AN-1084 Parallel Application of Link Chips
- AN-1085 FPD-Link PCB and Interconnect Design-In Guidelines
- AN-1127 LVDS Display Interface (LDI) TFT Data Mapping for Interoperability with FPD-Link
- AN-1163 TFT Data Mapping for Dual Pixel LDI Application - Alternate A - Color Map

Interface Applications Hotline:

The Interface Hotline number is: +1 408 721-8500

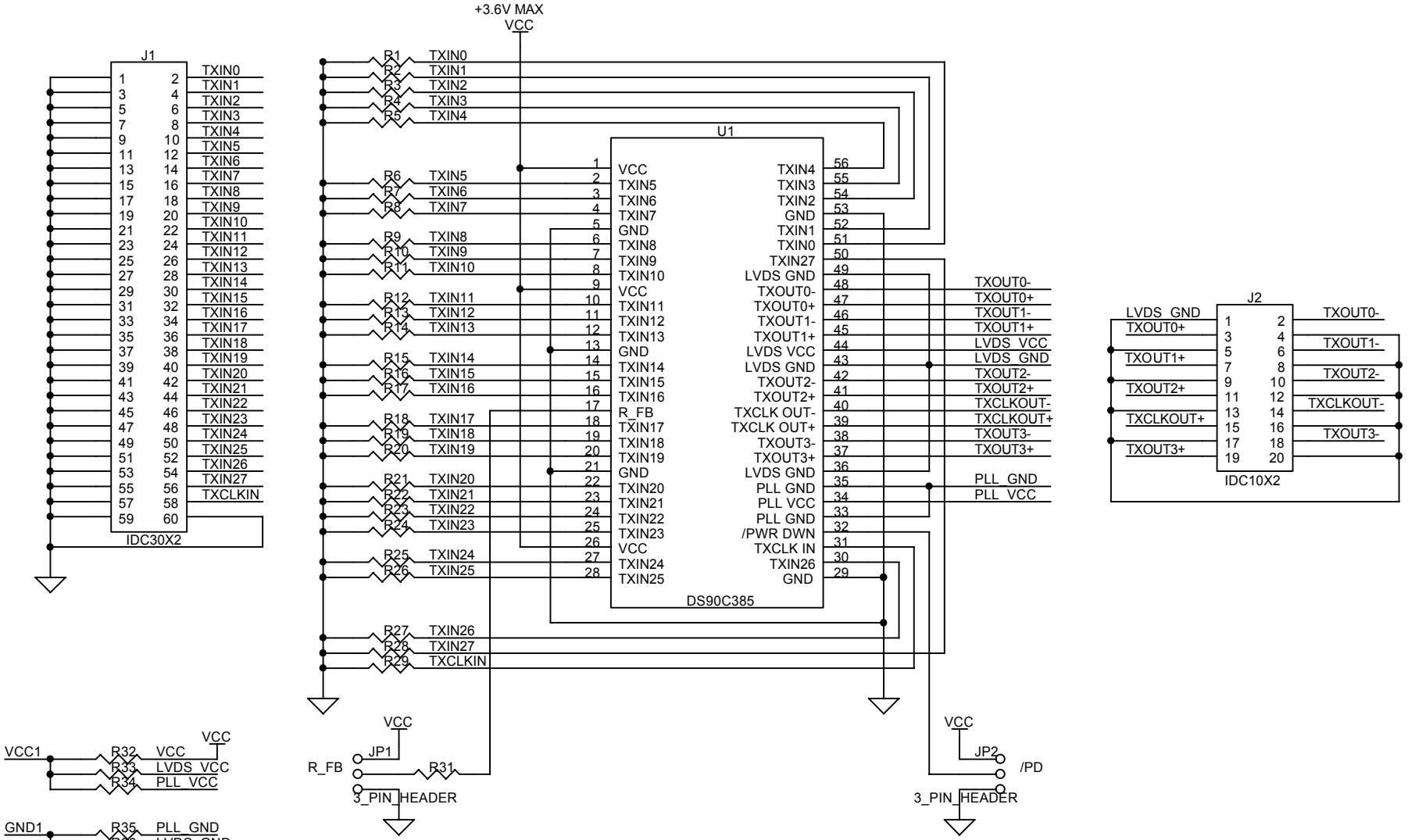
Appendix

Tx PCB Schematic

Transmitter Board: HSL Demo Board Schematic
Document Number: HSL8TXR3
Rev: 3.0

Rx PCB Schematic

Receiver Board: HSL Demo Board Schematic
Document Number: HSL8RXR3
Rev: 3.0



National Semiconductor		
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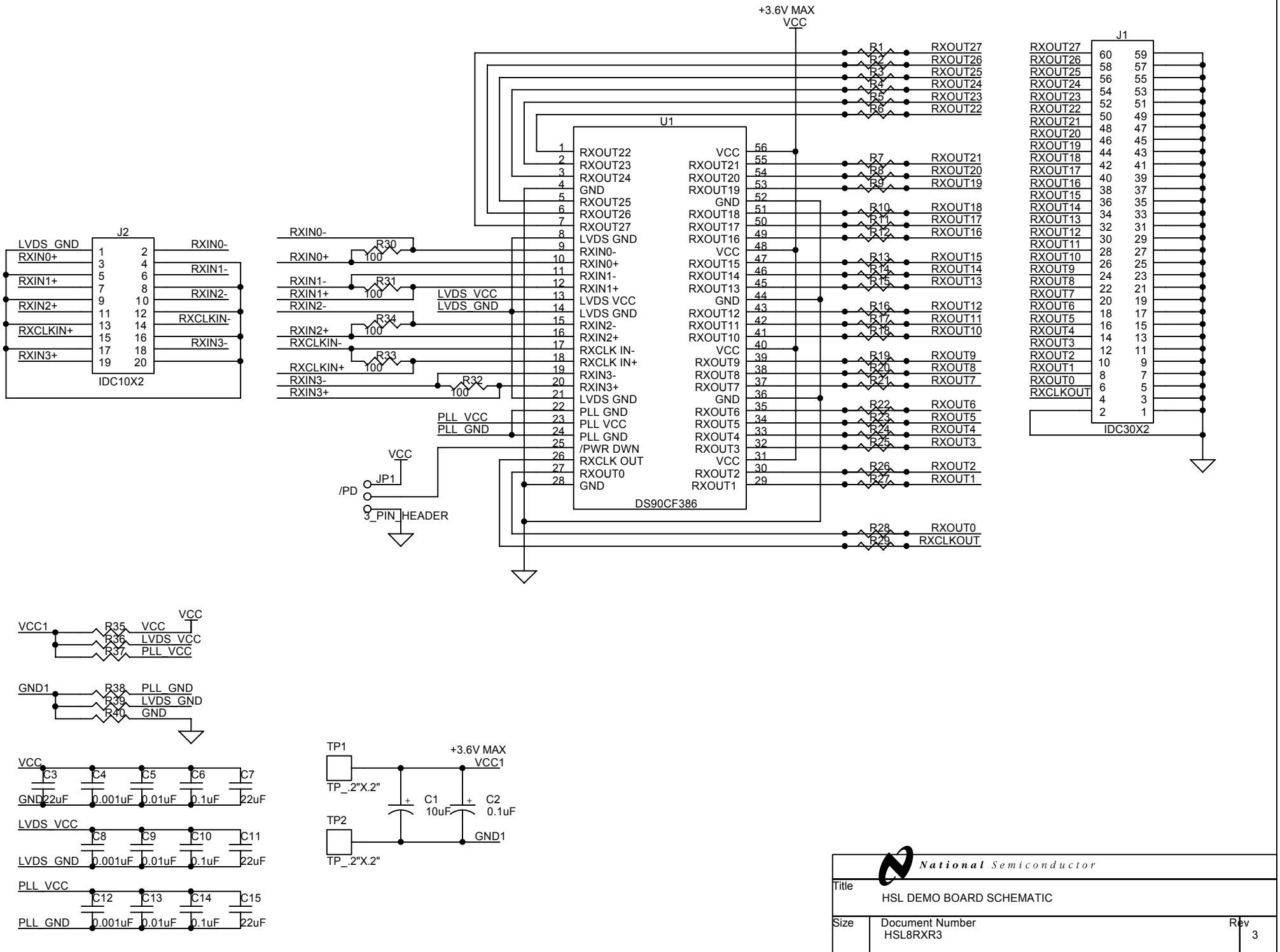
Size	Document Number HSL8TXR3	Rev 3
Date: Friday, September 22, 2000	Sheet 1 of 1	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VCC
U1
DS90CF386
J1
IDC30X2
J2
IDC10X2
JP1
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VCC1
GND1
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TP2
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C7 22uF
C8 0.001uF
C9 0.01uF
C10 0.1uF
C11 22uF
C12 0.001uF
C13 0.01uF
C14 0.1uF
C15 22uF
R30 100
R31 100
R32 100
R33 100
R34 100
R35 VCC
R36 LVDS_VCC
R37 PLL_VCC
R38 PLL_GND
R39 LVDS_GND
R40 GND
RXIN0-
RXIN0+
RXIN1-
RXIN1+
RXIN2-
RXIN2+
RXCLKIN-
RXCLKIN+
RXIN3-
RXIN3+
RXCLKOUT
/PD
National Semiconductor
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Sheet 1 of 1